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L Number	Hits	Search Text	DB	Time stamp
1	1	6263448.pn.	USPAT; EPO; JPO	2001/11/19 04:35
-	442	713/501.ccls.	USPAT; EPO; JPO	2001/11/19 04:34
-	311	713/322.ccls.	USPAT; EPO; JPO	2001/11/17 19:48
-	709	713/501.ccls. or 713/322.ccls.	USPAT; EPO; JPO	2001/11/17 19:49
-	5094	during adj active	USPAT; EPO; JPO	2001/11/17 19:49
-	18	(713/501.ccls. or 713/322.ccls.) and (during adj active)	USPAT; EPO; JPO	2001/11/17 20:01
-	1341	clock adj divider	USPAT; EPO; JPO	2001/11/17 20:02
-	52	(clock adj divider) and (713/501.ccls. or 713/322.ccls.)	USPAT; EPO; JPO	2001/11/17 20:02
-	7	((clock adj divider) and (713/501.ccls. or 713/322.ccls.)) and (during adj active)	USPAT; EPO; JPO	2001/11/17 20:04
-	2010	memory adj clock	USPAT; EPO; JPO	2001/11/17 20:04
-	18	(memory adj clock) and (clock adj divider)	USPAT; EPO; JPO	2001/11/17 20:05
-	7	5675808.URPN.	USPAT; EPO; JPO	2001/11/17 20:32
-	67	("4061933" | "4317180" | "4317221" | "4746899" | "4780843" | "4800524" | "4823312" | "4918339" | "5025387" | "5086387" | "5124579" | "5140679" | "5167024" | "5189647" | "5199105" | "5218239" | "5233309" | "5247655" | "5280595" | "5287457" | "5287470" | "5287525" | "5289584" | "5299315" | "5336939" | "5388265" | "5392437" | "5428765" | "5430393" | "5446403" | "5452401" | "5452434" | "5454114" | "5457801" | "5461266" | "5461652" | "5467042").PN.	USPAT; EPO; JPO	2001/11/17 20:43
-	29	5452401.URPN.	USPAT; EPO; JPO	2001/11/17 20:49

(12) United States Patent
Tsern et al.

(10) Patent No.: US 6,263,448 B1
(45) Date of Patent: Jul. 17, 2001

(54) **POWER CONTROL SYSTEM FOR SYNCHRONOUS MEMORY DEVICE**

(75) Inventors: Ely K. Tsern, Los Altos; Richard M. Barth, Palo Alto; Craig E. Hampel, San Jose; Donald C. Stark, Los Altos, all of CA (US)

(73) Assignee: Rambus Inc., Los Altos, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/169,378

(22) Filed: Oct. 9, 1998

Related U.S. Application Data

(60) Provisional application No. 60/061,664, filed on Oct. 10, 1997.

(51) Int. Cl.[7] G06F 1/04

(52) U.S. Cl. 713/501; 713/600

(58) Field of Search 713/501, 500, 713/600, 300, 322, 502, 503; 712/219

(56) **References Cited**

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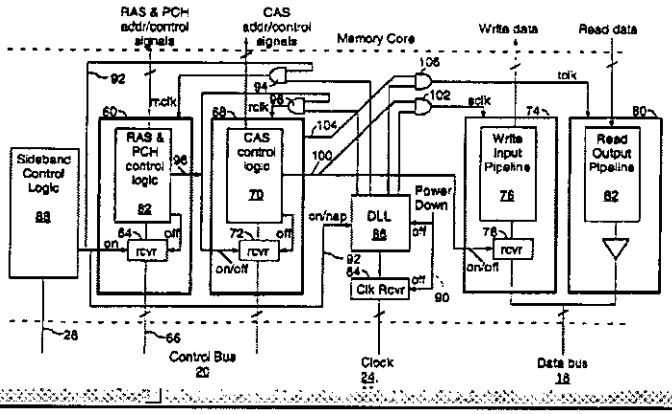
Primary Examiner—Thomas Black
Assistant Examiner—Mary Wang
(74) *Attorney, Agent, or Firm*—Pennie & Edmonds LLP

(57) **ABSTRACT**

A memory device with multiple clock domains. Separate clocks to different portions of the control circuitry create different clock domains. The different domains are sequentially turned on as needed to limit the power consumed. The turn on time of the domains is overlapped with the latency for the memory access to make the power control transparent to the user accessing the memory core. The memory device can dynamically switch between a fast and a slow clock depending upon the needed data bandwidth. The data bandwidth across the memory interface can be monitored by the memory controller, and when it drops below a certain threshold, a slower clock can be used. The clock speed can be dynamically increased as the bandwidth demand increases.

35 Claims, 9 Drawing Sheets



+384* 44.1 1 1 0 48.0 33.075 1 1 1 9.6 6.62 PCS yback Crystal Select When high, the 16.9344 MHz crystal oscillator (XTAL2) is used for the playb sample frequency. When low, the 24.576 MHz crystal oscillator (XTAL1) is

used.

DETL:

##STR44## RDF[2:0] Rec Selection. These three bits specify the record data format for the CODEC. These bits are accessible in Modes 2 and 3 only. Bits 2 1 0 Format 0 0 0 8-bit unsigned 0 0 1 .mu.-Law 0 1 0 16-bit-signed, little endian 0 1 1 A-Law 1 0 0 Reserved, default to 8-bit unsigned 1 0 1 IMA-compliant ADPCM 1 1 0 16-Bit signed, big endian .1 1 1 Reserved, default to 8-bit unsigned RSM Record Stereo/Mono Select. When high, stereo operation is selected; sampl will alternate left then right. When low, mono mode is selected; record samples come only from the left ADC. This bit is accessible in modes 2 and only. RCD[2:0] Record Clock Divider Select. These three bits specify the record clock rate. These bits are accessible from mode 3 only; in mode 2, these bits are reserved. *These divide-downs are provided to function when XTAL1 is less than 18.5 MHz. Sampling Rate (kilohertz) Bits 3 2 1 24.5 MH XTAL 16.9 MHz XTAL 0 0 0 8.0 5.51 0 0 1 16.0 11.025 0 1 0 27.42 18.9 0 32.0 22.05 1 0 0 +448* 37.8 1 0 1 +384* 44.1 1 1 0 48.0 33.075 1 1 1 9.6 6.62 RCS Record Crystal Select. When high, the 16.9344 MHz crystal oscil is used. When low, the 24.576 MHz crystal oscillator is used. This bit is accessible from mode 3 only; in mode 2, this bit is reserved.

CLPV:

wherein said clock distribution circuit further comprises an external memory clock selection circuit for selectively providing said memory interface circuit with the low-frequency clock signal in response to the circuit shut-down signal.

CLPV:

wherein said clock distribution circuit further comprises an external memory clock selection circuit for providing said memory interface circuit with the low-frequency clock signal in response to the suspend mode signal.

United States Pat (19)

Gulick et al.

[11] Patent Number: 5,675,808

[45] Date of Patent: Oct. 7, 1997

[54] **POWER CONTROL OF CIRCUIT MODULES WITHIN AN INTEGRATED CIRCUIT**

[75] Inventors: Dale E. Gulick; Larry D. Hewitt; Michael Hogan; David Norris, all of Austin, Tex.

[73] Assignee: Advanced Micro Devices, Inc., Sunnyvale, Calif.

[21] Appl. No.: 333,537

[22] Filed: Nov. 2, 1994

[51] Int. Cl.* G06F 1/32

[52] U.S. Cl. 395/750; 364/707; 364/273.1; 364/273.2; 364/232.8; 364/DIG. 1

[58] Field of Search 395/250, 550, 395/800, 428, 750; 364/707; 365/226, 227; 307/66; 327/291, 299

[56] References Cited

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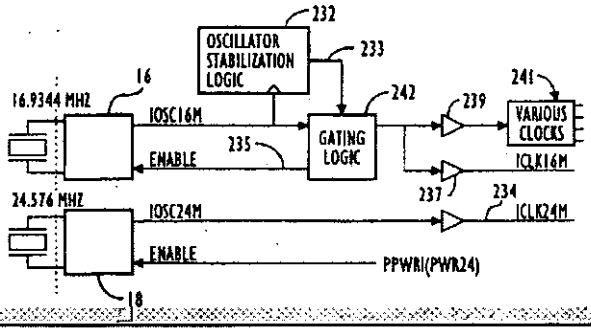
Primary Examiner—Gopal C. Ray

Attorney, Agent, or Firm—Fulbright & Jaworski LLP

[57] **ABSTRACT**

A power control and memory refresh rate management circuit is described. The power control circuit provides circuitry for selectively disabling or enabling modular logic circuit blocks within a VLSI integrated circuit under program control from an external processor, or for suspended circuit operation in general. In low-power modes external memory refresh signal generation circuits are provided with a low-frequency oscillator signal to conserve power.

13 Claims, 135 Drawing Sheets



US-PAT-NO: 5452401
DOCUMENT-IDENTIFIER: US 5452401 A
TITLE: Selective power-down for high performance CPU/system
DATE-ISSUED: September 19, 1995
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Chong M.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 713/322

ABSTRACT:
A microelectronic device according to the present invention is made up of two or more functional units, which are all disposed on a single chip, or die. The present invention works on the strategy that all of the functional units on the die are not, and do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device. The present invention on a very rapid basis (typically a half clock cycle), therefore, turns on and off the functional units of the microelectronic device in accordance with the requirements of the program being executed. This power down can be achieved by one of three techniques; turning off clock inputs to the functional units, interrupting the supply of power to the functional units, or deactivating input signals to the functional units. The operation of the present invention results in a very significant reduction in power consumption and corresponding heat dissipation by the microelectronic device as compared to the conventional approach of keeping all functional units operational all of the time.

18 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

SELECTIVE POWER-DOWN FOR HIGH PERFORMANCE CPU/SYSTEM

Inventor: Chong M. Lin, Sunnyvale, Calif.

Assignee: Seiko Epson Corporation, Tokyo, Japan

Appl. No.: 860,717

Filed: Mar. 31, 1992

Int. Cl.[6] G06F 9/34
U.S. Cl. 395/750; 364/DIG. 1
Field of Search 395/375, 425, 550, 575, 395/800; 235/152; 331/143

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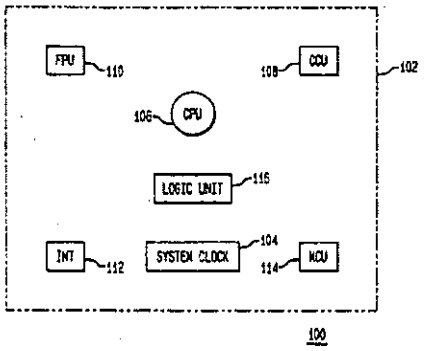
Primary Examiner—Allen R. MacDonald
Assistant Examiner—Tariq Hafiz
Attorney, Agent, or Firm—Sterne, Kessler, Goldstein & Fox

[57] ABSTRACT

A microelectronic device according to the present invention is made up of two or more functional units, which are all disposed on a single chip, or die. The present invention works on the strategy that all of the functional units on the die are not, and do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device. The present invention on a very rapid basis (typically a half clock cycle), therefore, turns on and off the functional units of the microelectronic device in accordance with the requirements of the program being executed. This power down can be achieved by one of three techniques; turning off clock inputs to the functional units, interrupting the supply of power to the functional units, or deactivating input signals to the functional units. The operation of the present invention results in a very significant reduction in power consumption and corresponding heat dissipation by the microelectronic device as compared to the conventional approach of keeping all functional units operational all of the time.

18 Claims, 7 Drawing Sheets



US-CL-CURRENT: 307/64,330/265 ,360/75 ,713/300 ,713/310 ,713/320 ,713 ,713/323

US-PAT-NO: 6314523
DOCUMENT-IDENTIFIER: US 6314523 B1
TITLE: Apparatus for distributing power to a system of independently powere devices
DATE-ISSUED: November 6, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Voltz; Christopher	Houston	TX	N/A	N/A

US-CL-CURRENT: 713/324,307/64 ,330/265 ,360/75 ,713/300 ,713/310 ,713 ,713/322 ,713/323

ABSTRACT:

According to the present invention, an apparatus having a plurality of independently operable and powerable devices is disclosed. The apparatus includes a plurality of power rails, a plurality of ground planes, and a power management circuit. One of the power rails is associated with one of the plurality of independently operable devices. One of the plurality of ground planes is selectively associated with one or more of the plurality of power rails. The power management circuit couples to the plurality of power rails and the second plurality of ground planes, for selectively deactivating at least one of the plurality of ground planes independently of any of the other plurality of power rails.

27 Claims, 9 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

(12) United States Patent
Voltz

(10) Patent No.: US 6,314,523 B1
(45) Date of Patent: *Nov. 6, 2001

(54) **APPARATUS FOR DISTRIBUTING POWER TO A SYSTEM OF INDEPENDENTLY POWERED DEVICES**

(75) Inventor: **Christopher Voltz**, Houston, TX (US)

(73) Assignee: **Compaq Computer Corporation**, Houston, TX (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 08/835,628

(22) Filed: Apr. 9, 1997

(51) Int. Cl.[7] G06F 1/26; G06F 1/28; G06F 1/30

(52) U.S. Cl. 713/324; 713/300; 713/310; 713/320; 713/322; 713/323; 360/75; 330/265; 307/64

(58) Field of Search 395/750.03, 750.02, 395/750.05, 750.06; 364/707; 713/300, 310, 320, 322, 324, 321, 323; 330/265; 307/64; 360/75

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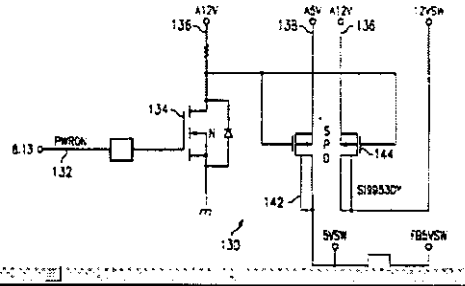
Primary Examiner—Ayaz Sheikh
Assistant Examiner—Frantz Jean
(74) *Attorney, Agent, or Firm*—Sharp, Comfort & Merrett, P.C.

(57) ABSTRACT

According to the present invention, an apparatus having a plurality of independently operable and powerable devices is disclosed. The apparatus includes a plurality of power rails, a plurality of ground planes, and a power management circuit. One of the power rails is associated with one of the plurality of independently operable devices. One of the plurality of ground planes is selectively associated with one or more of the plurality of power rails. The power management circuit couples to the plurality of power rails and the second plurality of ground planes, for selectively deactivating at least one of the plurality of ground planes independently of any of the other plurality of power rails.

27 Claims, 5 Drawing Sheets



Selective power down.

US-CL-CURRENT: 713/321,713/322

US-PAT-NO: 5502689
DOCUMENT-IDENTIFIER: US 5502689 A
TITLE: Clock generator capable of shut-down mode and clock generation m
DATE-ISSUED: March 26, 1996
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Peterson; Joseph W.	Austin	TX	N/A	N/A
Hendrickson; Alan F.	Austin	TX	N/A	N/A
Gulick; Dale E.	Austin	TX	N/A	N/A
Grumlose; Dean	Austin	TX	N/A	N/A

US-CL-CURRENT: 368/156,713/321 ,713/322
ABSTRACT:
A clock generator and interrupt bypass circuit for use in reducing the power consumption of the electrical system in which they are implemented. The clo generator provides module clock signals for sequencing modules within the s electrical system, and is capable of generating those module clock signals wh in an active mode, and of not generating those module clock signals when in stand-by mode. The clock generator is further capable of providing a delay o a predetermined length from a request to enter shut-down mode to actual ent into shut-down mode, allowing time to prepare the electrical system for shut-down mode. The interrupt bypass circuit provides a means of leaving shut-down mode in the event that the relevant interrupt requests have been masked.
9 Claims, 9 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

United States Patent [19]
Peterson et al.
[11] Patent Number: 5,502,689
[45] Date of Patent: Mar. 26, 1996

[54] **CLOCK GENERATOR CAPABLE OF SHUT-DOWN MODE AND CLOCK GENERATION METHOD**

[75] Inventors: Joseph W. Peterson; Alan F. Hendrickson; Dale E. Gulick; Dean Grumlose, all of Austin, Tex.

[73] Assignee: Advanced Micro Devices, Inc., Sunnyvale, Calif.

[21] Appl. No.: 201,077

[22] Filed: Feb. 24, 1994

Related U.S. Application Data

[63] Continuation of Ser. No. 918,622, Jul. 21, 1992, abandoned.

[51] Int. Cl.[6] G04F 5/00; G06F 1/00

[52] U.S. Cl. 368/156; 364/707; 395/750

[58] Field of Search 368/10, 66, 155–157, 368/200–204; 364/707; 395/750

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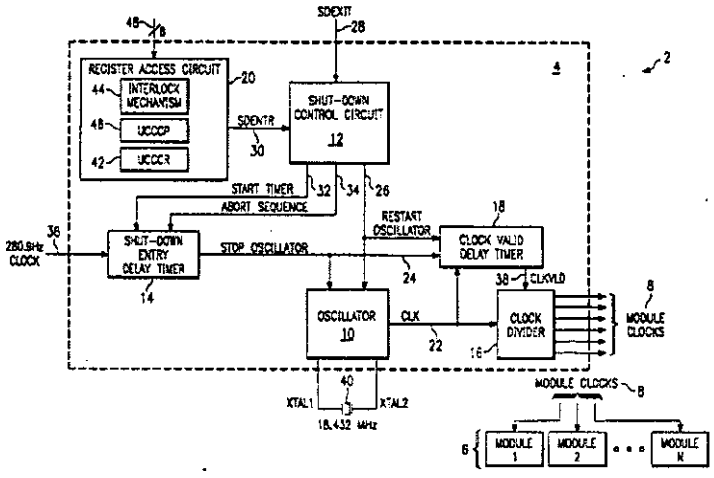
2080585	2/1982	United Kingdom .
8802017	6/1983	WIPO .

Primary Examiner—Vit W. Miska
Attorney, Agent, or Firm—Jenkens & Gilchrist

[57] ABSTRACT

A clock generator and interrupt bypass circuit for use in reducing the power consumption of the electrical system in which they are implemented. The clock generator provides module clock signals for sequencing modules within the same electrical system, and is capable of generating those module clock signals when in an active mode, and of not generating those module clock signals when in a stand-by mode. The clock generator is further capable of providing a delay of a predetermined length from a request to enter shut-down mode to actual entry into shut-down mode, allowing time to prepare the electrical system for shut-down mode. The interrupt bypass circuit provides a means of leaving shut-down mode in the event that the relevant interrupt requests have been masked.

9 Claims, 7 Drawing Sheets



US-PAT-NO: 5815692
DOCUMENT-IDENTIFIER: US 5815692 A
TITLE: Distributed clock generator
DATE-ISSUED: September 29, 1998
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
McDermott; Mark W.	Austin	TX	N/A	N/A

US-CL-CURRENT: 713/501

ABSTRACT:

A processor includes a distributed clock generator employing a plurality of independently adjustable clocks reconstituted locally from multiple signals. A centralized generator is disposed substantially in the middle of the processing system with satellite reconstitutors being disposed around the periphery to service various functional units which collectively manifest the processing system. The distribution of the multiple signals to the satellite reconstitutors provides substantially equal wire length and local reconstitution mitigates R-C time constant skew problems.

5 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 18

United States Patent [19]
McDermott

[11] Patent Number: 5,815,692
[45] Date of Patent: *Sep. 29, 1998

DISTRIBUTED CLOCK GENERATOR

Inventor: Mark W. McDermott, Austin, Tex.

Assignee: National Semiconductor Corporation, Santa Clara, Calif.

Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Appl. No.: 572,947

Filed: Dec. 15, 1995

Int. Cl.[6] G06F 1/06
U.S. Cl. 395/556
Field of Search 395/556, 558

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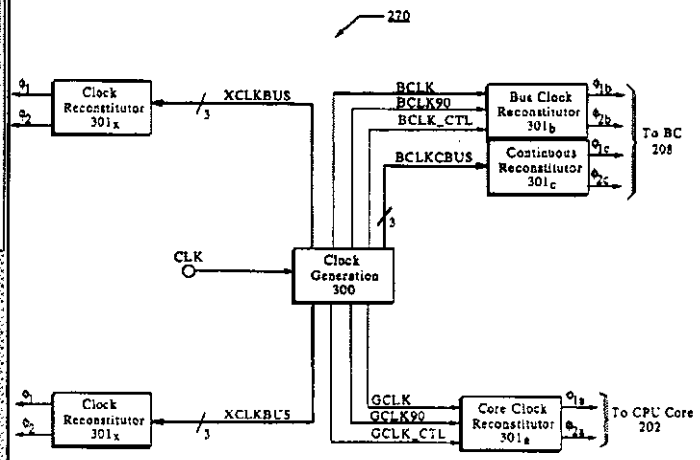
Primary Examiner—Thomas M. Heckler
Attorney, Agent, or Firm—John L. Maxin

[57] ABSTRACT

A processor includes a distributed clock generator employing a plurality of independently adjustable clocks reconstituted locally from multiple signals. A centralized generator is disposed substantially in the middle of the processing system with satellite reconstitutors being disposed around the periphery to service various functional units which collectively manifest the processing system. The distribution of the multiple signals to the satellite reconstitutors provides substantially equal wire length and local reconstitution mitigates R-C time constant skew problems.

5 Claims, 18 Drawing Sheets



DOCUMENT-IDENTIFIER: US 6301671 B1
TITLE: Apparatus and method for power reduction control in a video encoder device

ABPL:
System for reducing power consumption in MPEG-2 compliant video encoder circuitry employs logic for controlling first clock signals input to functional I, HSU and RSU blocks and functional sub-units performing specific tasks therein. Second clock signals are continuously input to a processing detection circuits requiring continuous clock inputs throughout video encode operations for a functional sub-unit. A trigger signal is asserted by the sub-unit itself or, an external processor, to indicate idle or active processing for that particular sub-unit. The combination of the second clock signals and receipt of the trigger signal enable the sub-unit to generate a sleep signal for that sub-unit which is input to a clock control circuit to either enable input of first clock signals to the functional sub-unit during active processing or, disable input of the first clock signal during idle, in-active processing periods, for as long as the trigger signal is asserted. There are a variety of video input conditions that may be detected which will enable generation of a trigger signal indicating idle processing for one or more functional sub-units, including, for example, detection of still input pictures, fade sequences and specification of high bitstream output rates.

DEPR:
FIG. 4 illustrates a generic functional sub-circuit 65 from a functional block, e.g., I block, HSU or RSU blocks. This functional sub-circuit 65 contains circuitry for implementing a specific function, hereinafter referred to as function "X" wherein "X"=1, . . . , n implements a specific task. As shown in FIG. 4, functional sub-circuit 65 typically comprises a first domain of circuitry 75 and a second domain of circuitry 77 that differ in the following manner: the first domain of circuitry 75 contains flip-flop, latch and/or other digital logic circuitry, e.g., counters, (depending upon the specific function) that require a continuous clock input, such as clock signal 22 as long as the functional I, HSU or RSU block is enabled. First domain circuitry 75 functions to detect pending processing conditions or completion of a particular processing task. The second domain circuitry 77 contains that processing circuitry specific to the particular function and will be enabled at various times, when required. Thus, in order to reduce power consumption, a clock input 26 need only be enabled during active processing of second domain circuitry.

DEPR:
As mentioned above, MPEG-2 encoder applications may typically involve a m estimation search function. In MPEG-2, this search is divided into two main

(12) United States Patent
Boice et al.
(10) Patent No.: US 6,301,671 B1
(45) Date of Patent: Oct. 9, 2001

(54) APPARATUS AND METHOD FOR POWER REDUCTION CONTROL IN A VIDEO ENCODER DEVICE

(75) Inventors: Charles Edward Boice; John Mark Kaczmarczyk, both of Endicott; John Ashley Murdock, Apalachin; Michael Patrick Vachon, Johnson City; Robert Leslie Woodard, Newark Valley, all of NY (US)

(73) Assignee: International Business Machines Corporation, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/046,287

(22) Filed: Mar. 23, 1998

(51) Int. Cl.[7] G06F 1/32
(52) U.S. Cl. 713/322; 713/601
(58) Field of Search 713/300, 320, 713/322, 324, 601

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(74) *Attorney, Agent, or Firm*—Scully, Scott, Murphy & Presser

(57) ABSTRACT

System for reducing power consumption in MPEG-2 compliant video encoder circuitry employs logic for controlling first clock signals input to functional I, HSU and RSU blocks and functional sub-units performing specific tasks therein. Second clock signals are continuously input to a processing detection circuits requiring continuous clock inputs throughout video encode operations for a functional sub-unit. A trigger signal is asserted by the sub-unit itself or, an external processor, to indicate idle or active processing for that particular sub-unit. The combination of the second clock signals and receipt of the trigger signal enable the sub-unit to generate a sleep signal for that sub-unit which is input to a clock control circuit to either enable input of first clock signals to the functional sub-unit during active processing periods, for as long as the trigger signal is asserted. There are a variety of video input conditions that may be detected which will enable generation of a trigger signal indicating idle processing for one or more functional sub-units, including, for example, detection of still input pictures, fade sequences and specification of high bitstream output rates.

27 Claims, 7 Drawing Sheets